IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.:
James Y.C. Chang	Art Unit: 2832
Appl. No. 09/493,942	Examiner: Donovan, L
Filed: 1/28/2000	Atty. Docket: 1875.1380006
For: Multi-Track Integrated Spiral Inductor	

Amendment And Reply Under 37 C.F.R. §1.116

Commissioner for Patents
Washington, D.C. 20231

Sir:

In reply to the Final Office Action dated **June 13, 2002**, (PTO Prosecution File Wrapper Paper No. 22), Applicants submit the following Amendment and Remarks. This Amendment is provided in the following format:

(A) A clean version of each replacement paragraph/section/claim along with clear instructions for entry;

(B) Starting on a separate page, appropriate remarks and arguments. 37 C.F.R. § 1.111 and MPEP 714; and

(C) Starting on a separate page, a marked-up version entitled: "Version with markings to show changes made."

It is not believed that extensions of time or fees for net addition of claims are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Kindly enter the following amendments:

1. (Twice Amended) An integrated circuit inductor comprising:

a substrate;

a spiral inductor metalization pattern disposed on the substrate including a plurality of parallel tracks in a spiral pattern each track having a first end and a second end and having the first ends coupled together and the second ends coupled together; and

a n+ diffusion layer disposed in the substrate directly underneath the spiral inductor metalization pattern.

10. (Twice Amended) The integrated circuit inductor of claim 1, in which the n^+ diffusion layer has a fingered pattern shape with n+ fingers electrically isolated by regions of polysilicon.

14. (Twice Amended) An integrated circuit inductor comprising:

a substrate having a first layer and a second layer;

a first track disposed on the first layer in a first spiral pattern and having a first input and a first output;

a second track disposed on the second layer in a second spiral pattern and having a second input and a second output, the second spiral pattern oriented parallel to the first spiral pattern; and

a pattern of via holes sufficient to couple a varying voltage present along the length of the first track on to the second track;

the first and second inputs connected together by a first via hole of the pattern of via holes, and the first and second outputs connected together by a second via hole of the pattern of via holes.